

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	((back near5 (substrate wafer)) and (mask resist pr (photo near3 resist)) and (trench recess hole open\$3 groove mesa) and etch\$3 and (conductive polysilicon metal) and (first near5 (diffusion impurity doped) near5 layer) and (second near5 (diffusion impurity doped) near5 layer) and (dopant polarity n-type p-type)). clm.	US-PGPU B	OR	ON	2005/10/22 10:12
L2	0	((back near5 (substrate wafer)) and (mask resist pr (photo near3 resist)) and (trench recess hole open\$3 groove mesa) and etch\$3 and (conductive polysilicon metal) and (first near5 (diffusion impurity doped) near5 layer) and (second near5 (diffusion impurity doped) near5 layer) and (dopant polarity n-type p-type) and (heat near5 (sink spreader dessipat\$3))). clm.	US-PGPU B	OR	ON	2005/10/22 10:17